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First Name = VICTOR

| Application#             | Patent#    | Status | Date Filed | Title  | Inventor Name 4 |
|--------------------------|------------|--------|------------|--|-----------------|
| <a href="#">60503713</a> | Not Issued | 020    | 09/15/2003 | SINGLE WIRE BUS FOR CONNECTING DEVICES - PROGRAMMING MODEL                                 | FLACHS, VICTOR  |
| <a href="#">60503450</a> | Not Issued | 020    | 09/15/2003 | SINGLE WIRE BUS FOR CONNECTING DEVICES   | FLACHS, VICTOR  |
| <a href="#">09850561</a> | Not Issued | 041    | 05/07/2001 | A/D CONVERTER WITH COMPARATORS AND LOW-POWER DETECTION MODE FOR RESISTIVE MATRIX KEYBOARDS | FLACHS, VICTOR  |
| <a href="#">09810746</a> | Not Issued | 071    | 03/16/2001 | SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR                   | FLACHS, VICTOR  |

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Your Search was:

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First Name = YUVAL

| Application#             | Patent#    | Status | Date Filed | Title   | Inventor Name 2  |
|--------------------------|------------|--------|------------|---|------------------|
| <a href="#">60505241</a> | Not Issued | 020    | 09/23/2003 | METHOD AND APPARATUS FOR BUS SWITCH CONTROL WITH FILTERING OF PRE-DEFINED TYPES OF TRANSACTIONS | KIRSCHNER, YUVAL |
| <a href="#">09810746</a> | Not Issued | 071    | 03/16/2001 | SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR                        | KIRSCHNER, YUVAL |

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**Inventor Name Search Result**

Your Search was:

Last Name = FRIEDMAN

First Name = YEHEZKEL

| Application#             | Patent#                 | Status | Date Filed | Title   | Inventor Name 3     |
|--------------------------|-------------------------|--------|------------|---|---------------------|
| <a href="#">09810746</a> | Not Issued              | 071    | 03/16/2001 | SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR  | FRIEDMAN, YEHEZKEL  |
| <a href="#">08813501</a> | <a href="#">5964853</a> | 150    | 03/07/1997 | INTERFACE CONTROLLER INCLUDING HARDWARE MECHANISM TO HANDLE PS/2 INTERFACE  | FRIEDMAN , YEHEZKEL |
| <a href="#">07642928</a> | <a href="#">5250940</a> | 150    | 01/18/1991 | MULTI-MODE HOME TERMINAL SYSTEM THAT UTILIZES A SINGLE EMBEDDED GENERAL PURPOSE/DSP PROCESSOR AND A SINGLE RANDOM ACCESS MEMORY | FRIEDMAN , YEHEZKEL |

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| Application#             | Patent#    | Status | Date Filed | Title   | Inventor Name 38 |
|--------------------------|------------|--------|------------|---|------------------|
| <a href="#">60505241</a> | Not Issued | 020    | 09/23/2003 | METHOD AND APPARATUS FOR BUS SWITCH CONTROL WITH FILTERING OF PRE-DEFINED TYPES OF TRANSACTIONS         | FALIK, OHAD      |
| <a href="#">60503713</a> | Not Issued | 020    | 09/15/2003 | SINGLE WIRE BUS FOR CONNECTING DEVICES - PROGRAMMING MODEL  | FALIK, OHAD      |
| <a href="#">60503450</a> | Not Issued | 020    | 09/15/2003 | SINGLE WIRE BUS FOR CONNECTING DEVICES  | FALIK, OHAD      |
| <a href="#">60455973</a> | Not Issued | 020    | 03/19/2003 | CLOCK FREQUENCY MONITOR   | FALIK, OHAD      |
| <a href="#">60422924</a> | Not Issued | 020    | 11/01/2002 | PC87591X-BASED DIRECT CD PLAYER (DCDP) FOR MOBILE COMPUTERS   | FALIK, OHAD      |
| <a href="#">60385478</a> | Not Issued | 159    | 06/03/2002 | EMBEDDED CONTROLLER BASED BIOS BOOT ROM SELECT  | FALIK, OHAD      |
| <a href="#">60137129</a> | Not Issued | 159    | 05/28/1999 | DIGITAL SIGNAL PROCESSOR AND METHOD FOR PRIORITIZED ACCESS BY MULTIPLE CORE PROCESSORS TO SHARED MEMORY | FALIK , OHAD     |
| <a href="#">60051943</a> | Not Issued | 159    | 07/08/1997 | MULTI-PROCESSOR ELEMENT PROVIDED WITH HARDWARE FOR SOFTWARE DEBUGGING                                   | FALIK , OHAD     |
| <a href="#">10735274</a> | Not Issued | 019    | 12/12/2003 | REGULATING DATA TRAFFIC IN A HIERARCHICAL TOKEN-BASED BUS SYSTEM  | FALIK, OHAD      |
| <a href="#">10699623</a> | Not Issued | 019    | 10/31/2003 | CONTROLLER-BASED DIRECT CONTENT DISK PLAYER FOR MOBILE COMPUTERS  | FALIK, OHAD      |
|                          |            |        |            |   |                  |

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|-----------------|----------------|-----|------------|---|-------------|
| <u>10699600</u> | Not Issued     | 019 | 10/31/2003 | CONTROLLER-BASED DIRECT CONTENT DISK PLAYER FOR MOBILE COMPUTERS  | FALIK, OHAD |
| <u>10699408</u> | Not Issued     | 019 | 10/31/2003 | CONTROLLER-BASED DIRECT CONTENT DISK PLAYER FOR MOBILE COMPUTERS  | FALIK, OHAD |
| <u>10698972</u> | Not Issued     | 019 | 10/31/2003 | CONTROLLER-BASED DIRECT CONTENT DISK PLAYER FOR MOBILE COMPUTERS  | FALIK, OHAD |
| <u>10453851</u> | Not Issued     | 020 | 06/03/2003 | EMBEDDED CONTROLLER BASED BIOS BOOT ROM SELECT  | FALIK, OHAD |
| <u>10389292</u> | Not Issued     | 092 | 03/13/2003 | SIGNAL ACTIVE PERCENTAGE MONITOR  | FALIK, OHAD |
| <u>10375929</u> | Not Issued     | 030 | 02/27/2003 | USING ACPI POWER BUTTON SIGNAL FOR REMOTELY CONTROLLING THE POWER OF A PC   | FALIK, OHAD |
| <u>10301831</u> | Not Issued     | 030 | 11/21/2002 | METHOD AND APPARATUS FOR SENSING TEMPERATURE  | FALIK, OHAD |
| <u>10115460</u> | Not Issued     | 030 | 04/02/2002 | SECURE LOCK MECHANISM BASED ON A LOCK WORD  | FALIK, OHAD |
| <u>09862986</u> | Not Issued     | 030 | 05/22/2001 | SECURE UNIVERSAL SERIAL BUS   | FALIK, OHAD |
| <u>09850561</u> | Not Issued     | 041 | 05/07/2001 | A/D CONVERTER WITH COMPARATORS AND LOW-POWER DETECTION MODE FOR RESISTIVE MATRIX KEYBOARDS                              | FALIK, OHAD |
| <u>09850543</u> | Not Issued     | 030 | 05/07/2001 | FLASH MEMORY PROTECTION SCHEME FOR SECURED SHARED BIOS IMPLEMENTATION IN PERSONAL COMPUTERS WITH AN EMBEDDED CONTROLLER | FALIK, OHAD |
| <u>09810746</u> | Not Issued     | 071 | 03/16/2001 | SHARING OF FUNCTIONS BETWEEN AN EMBEDDED CONTROLLER AND A HOST PROCESSOR  | FALIK, OHAD |
| <u>09579258</u> | <u>6532507</u> | 150 | 05/25/2000 | DIGITAL SIGNAL PROCESSOR AND METHOD FOR PRIORITIZED ACCESS BY MULTIPLE CORE PROCESSORS TO SHARED                        | FALIK, OHAD |

|                 |                |     |            | DEVICE   |             |
|-----------------|----------------|-----|------------|--|-------------|
| <u>09469663</u> | <u>6173355</u> | 150 | 12/22/1999 | SYSTEM FOR SENDING AND RECEIVING DATA ON A UNIVERSAL SERIAL BUS (USB) USING A MEMORY SHARED AMONG A NUMBER OF ENDPOINTS                    | FALIK, OHAD |
| <u>09096402</u> | <u>6065078</u> | 150 | 06/11/1998 | MULTI-PROCESSOR ELEMENT PROVIDED WITH HARDWARE FOR SOFTWARE DEBUGGING  | FALIK, OHAD |
| <u>09004003</u> | <u>6145045</u> | 150 | 01/07/1998 | SYSTEM FOR SENDING AND RECEIVING DATA ON A UNIVERSAL SERIAL BUS (USB) USING A MEMORY SHARED AMONG A NUMBER OF ENDPOINTS                    | FALIK, OHAD |
| <u>08993795</u> | Not Issued     | 161 | 12/18/1997 | PROCESSOR CORE WHICH PROVIDES A LINEAR EXTENSION OF AN ADDRESSABLE MEMORY SPACE  | FALIK, OHAD |
| <u>08889796</u> | <u>6263425</u> | 150 | 07/08/1997 | CIRCUIT THAT IMPLEMENTS SEMAPHORES IN A MULTIPROCESSOR ENVIRONMENT WITHOUT RELIANCE ON ATOMIC TEST AND SET OPERATIONS OF THE PROCESS CORES | FALIK, OHAD |
| <u>08821416</u> | <u>5822779</u> | 150 | 03/21/1997 | MICROPROCESSOR-BASED DATA PROCESSING APPARATUS THAT COMMENCES A NEXT OVERLAPPING CYCLE WHEN A READY SIGNAL IS DETECTED NOT TO BE ACTIVE    | FALIK, OHAD |
| <u>08813501</u> | <u>5964853</u> | 150 | 03/07/1997 | INTERFACE CONTROLLER INCLUDING HARDWARE MECHANISM TO HANDLE PS/2 INTERFACE   | FALIK, OHAD |
| <u>08708786</u> | <u>5915266</u> | 150 | 09/09/1996 | PROCESSOR CORE WHICH PROVIDES A LINEAR EXTENSION OF AN ADDRESSABLE MEMORY SPACE  | FALIK, OHAD |
| <u>08416489</u> | Not Issued     | 166 | 04/04/1995 | BUS OF CPU CORE OPTIMIZED FOR ACCESSING ON-CHIP  | FALIK, OHAD |

|                 |                |     |            |  |              |
|-----------------|----------------|-----|------------|--|--------------|
|                 |                |     |            | MEMORY DEVICES   |              |
| <u>08410113</u> | Not Issued     | 166 | 03/24/1995 | PROCESSOR CORE WHICH PROVIDES A LINEAR EXTENSION OF AN ADDRESSABLE MEMORY SPACE  | FALIK , OHAD |
| <u>08409742</u> | Not Issued     | 161 | 03/24/1995 | PROCESSOR CORE THAT FORMS ADDRESSES FROM PORTIONS OF THE ADDRESSES STORED IN MULTIPLE REGISTER MEANS WITHOUT PERFORMING ANY ARITHMETIC ON THE PORTIONS | FALIK , OHAD |
| <u>08248768</u> | <u>5566308</u> | 150 | 05/25/1994 | PROCESSOR CORE WHICH PROVIDES A LINEAR EXTENSION OF AN ADDRESSABLE MEMORY SPACE  | FALIK , OHAD |
| <u>08098203</u> | <u>5600821</u> | 150 | 07/28/1993 | DISTRIBUTED DIRECTORY FOR INFORMATION STORED ON AUDIO QUALITY MEMORY DEVICES   | FALIK , OHAD |
| <u>07989219</u> | <u>5446909</u> | 150 | 12/11/1992 | BINARY MULTIPLICATION IMPLEMENTED BY EXISTING HARDWARE WITH MINOR MODIFICATIONS TO SEQUENTIALLY DESIGNATE BITS OF THE OPERAND                          | FALIK , OHAD |
| <u>07989217</u> | Not Issued     | 166 | 12/11/1992 | BUS OF CPU CORE OPTIMIZED FOR ACCESSING ON-CHIP MEMORY DEVICES   | FALIK , OHAD |

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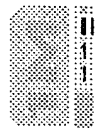
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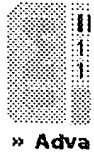


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**1** Memory data organization for improved cache performance in 99%



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Preeti Ranjan Panda , Nikil D. Dutt , Alexandru Nicolau

**ACM Transactions on Design Automation of Electronic Systems (TODAES)** October 1997

Volume 2 Issue 4

Code generation for embedded processors opens up the possibility for several performance optimization techniques that have been ignored by traditional compilers due to compilation time constraints. We present techniques that take into account the parameters of the data caches for organizing scalar and array variables declared in embedded code into memory, with the objective of improving data cache performance. We present techniques for clustering variables to minimize compulsory cache misse ...

**2** Graph-based code selection techniques for embedded processors 97%



**ACM Transactions on Design Automation of Electronic Systems (TODAES)** October 2000

Volume 5 Issue 4

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embedded processor applications

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**Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design** November 1992
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Theo Ungerer , Borut Robič , Jurij Šilc

**ACM Computing Surveys (CSUR)** March 2003

Volume 35 Issue 1

Hardware multithreading is becoming a generally applied technique in the next generation of microprocessors. Several multithreaded processors are announced by industry or already into production in the areas of high-performance microprocessors, media, and network processors. A multithreaded processor is able to pursue two or more threads of control in parallel within the processor pipeline. The contexts of two or more threads of control are often stored in separate on-chip register sets. Unused i ...
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- 1** Synthesis fo the hardware/software interface in microcontroller-based systems 97%

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- 2** A survey of processors with explicit multithreading 96%

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**ACM Computing Surveys (CSUR)** March 2003  
 Volume 35 Issue 1  
 Hardware multithreading is becoming a generally applied technique in the next generation of microprocessors. Several multithreaded processors are announced by industry or already into production in the areas of high-performance microprocessors, media, and network processors. A multithreaded processor is able to pursue two or more threads of control in parallel within the processor pipeline. The contexts of two or more threads of control are often stored in separate on-chip register sets. Unused i ...
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